REMARKS

Claims 2-5 and 10 are objected to as being dependent upon a rejected base claim. Claims 12-14 are similarly indicated as being allowable if, in addition to amending the claims to include the limitations of the base claim, the claims are also amended to address the 35 USC §101 and §112 rejections. No amendments are made to claims 1-10 because the base claims are thought to be allowable. Claim 11 is amended for purposes of clarification only and not for purposes of patentability. Claims 1-14 remain for consideration. Reconsideration and allowance are requested because all claims are thought to be allowable over the cited art.

The rejection of claims 11-14 under 35 USC 112, second paragraph, as being incomplete for omitting essential elements is respectfully traversed. Claim 11 includes limitations of and related to "a system-level simulation environment configured to ..." perform various functions. These limitations are thought to be understood by those skilled in the art to implicitly include a computing arrangement for performing the stated functions. Thus, no amendment is thought to be needed for compliance with §112. Claim 11 is amended, however, to clarify the limitations and for purposes of expediting prosecution.

The rejection of claims 11-14 under 35 USC §101 is respectfully traversed. The rejection should be withdrawn for the reasons set forth above in response to the rejection under §112.

The Office Action does not establish that claims 1, 6-9 and 11 are anticipated under 35 USC 102(b) by "Krukowski" ("Simulink/Matlab-to-VHDL Route for Full-Custom/FPGA Rapid Prototyping of DSP Algorithms" by Krukowski et al.). The rejection is respectfully traversed because the Office Action does not show that all the limitations of the claims are taught by Krukowski.

Claim 1, for example, includes limitations of and related to providing a plurality of hardware-level design objects, each hardware-level design object configured to generate a hardware definition of a hardware-level function, wherein one or more hardware-level design objects are combinable to implement each system-level design object. The limitations further include simulating behavior of a system-level design consistent with the system-level functions and behavior of a hardware definition from

the hardware-level design objects that implement the user-selected ones of the system-level design objects. These limitations are not shown to be suggested by Kurkowski.

The Office Action generally alleges that Kurkowski's pages 1 and 4-9 teach these limitations. However, no specific elements of Kurkowski are cited as corresponding to the specific limitations. The teachings of pages 1-9 appear to teach a different approach for creating a circuit design as compared to that which is claimed. Kurkowski, on page 4, column 1, in the first two full paragraphs, teaches conversion from Simulink to VHDL in two passes. In the first pass common blocks of the model are identified for generating separate VHDL files. In the second pass, Kurkowski's algorithm looks recursively through the model hierarchy creating the structural description of each block found in the first pass. There is no apparent correspondence to the claim limitations of a plurality of hardware design objects (which are distinct from the system-level design objects), with each hardware design object configured to generate a hardware definition of a hardware-level function and one or more of the hardware design objects are combinable to implement a system-level design object. An explanation of those specific elements taught by Kurkowski thought to correspond to the claim limitations is respectfully requested if the rejection is maintained. Otherwise, the rejection should be withdrawn because Kurkowski is not shown to teach all the limitations of the claims.

Claims 9 and 11 include similar functional limitations and are not shown to be unpatentable over Kurkowski for at least the reasons set forth above for claim 1.

The Office Action further fails to show that Kurkowski teaches all the limitations of claims 6-8. Claim 6 includes further limitations of simulating behavior of the design defined in the system-level design file with user-specified input-data generators that generate system-level input data; capturing the system-level input data generated by the input-data generators; and generating a hardware definition for a first testbench component that provides the system-level input data as input data to the hardware definitions. Kurkowski is not show to teach these limitations at the cited pages 9-10. In the cited portion, Kurkowski teaches a separate test bench that compares the results of VHDL simulation with the output from the Simulink model. There is no

apparent correspondence to the limitations of generating a hardware definition of a testbench component that provides the system-level input data as input data to the hardware definition. An explanation of those specific elements taught by Kurkowski thought to correspond to the claim limitations is respectfully requested if the rejection is maintained. Otherwise, the rejection should be withdrawn because Kurkowski is not shown to teach all the limitations of claim 6.

Claims 7 and 8 depend from claim 6 and are not shown to be anticipated for at least the reasons set forth above for claim 6.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patent, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 23, 2005.

Pat Slaback
Name

Signature